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PATENT APPLICATION
ATTORNEY DOCKET NO. Q56320

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kaoru NARITA

Appln. No.: 09/421,273

Group Art Unit: 2823

Confirmation No.: 3894

Examiner: J. Garcia

Filed: October 20, 1999

For: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

SUBMISSION OF FORMAL DRAWINGS

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith please find eleven (11) sheets of Formal Drawings. The submitted Formal Drawings are identical to the drawings submitted to the Patent Office on October 20, 1999, and no new matter has been incorporated into the Formal Drawings. Applicant is again furnishing another set of Formal Drawings to avoid abandonment of the instant application and to avoid unnecessary extension fees. The Examiner is respectfully requested to acknowledge receipt of these Formal Drawings.

In the Office Action dated May 6, 2002, the Examiner again requests that Applicant furnish drawings to facilitate the understanding of the invention, in compliance with 37 C.F.R. § 1.81. Contrary to the Examiner's statement, Applicant has furnished drawings on October 20, 1999 and

November 30, 2001 that are in compliance with 37 C.F.R. § 1.81, and that do provide an understanding of the invention.

In the Office Action, the Examiner states that "shallow trench isolating regions having a first depth, and provided in surface portions of said semiconductor substrate for defining active areas therebetween" are not depicted in the drawings. *See* page 2, first paragraph of the Office Action dated May 6, 2002.

Referring to Figure 5 of the instant application, as one example of an embodiment of the invention, it is plainly evident that shallow trench isolating regions 13/16 are disposed inside heavily doped n-type region 15, and the shallow trench isolating regions 13/16 penetrate to the p-type well 12. Active areas, e.g., the heavily doped n-type source/drain regions 17a/17b, are disposed in the p-type well 12, and are positioned between the shallow trench isolating regions 13/16. *See, e.g.,* Fig. 5 and page 10, lines 4-10 of the instant application.

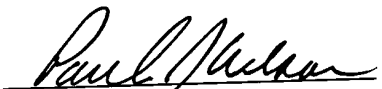
In addition, the Examiner further states that "a circuit component of an integrated circuit provided in one of said active areas, and connected between said terminal and a first source of constant voltage" is not depicted in the drawings. *See* page 2, first paragraph of the Office Action dated May 6, 2002.

Again, referring to Figure 5 of the instant application, a terminal 1 is connected to an active area 17a, and the other active area 17b is coupled to a source of constant voltage. In Figure 5, this source of constant voltage is a ground potential. *See* Fig. 5 and page 10, line 23 to page 11, line 4 of the instant application. In one embodiment of the present invention, the circuit component is a

field effect transistor 3 disposed over the active areas 17a/17b. *See* Fig. 5, page 9, lines 7-9 and page 11, lines 4-7 of the instant application.

Thus, Applicant believes that the Formal Drawings filed on October 20, 1999 and November 30, 2001 adequately facilitate the understanding of the invention.

Respectfully submitted,



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